Notice of Allowability	Application No.	Applicant(s)	
	09/587,496	BAILEY ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 1/20/2006*.

2. ☒ The allowed claim(s) is/are *5-8,11-13,15-17,19 and 27-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. Claims 5-8, 11-13, 15-17, 19, and 27-42 of U.S. Application 09/587,496, originally filed on 06/02/2000, are currently pending.

Drawings

2. The new drawings filed on 1/20/2006 overcome the objections to the drawings submitted on 06/02/0000.

Examiner's Statement of Reasons for Allowance

3. Claims 5-8, 11-13, 15-17, 19, and 27-42 are allowed.
4. Claims 5-8, 11-13, 15-17, 19, 27 and 31-32 were previously objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims.
5. In the After-Final Amendment filed on 1/20/2006, the Applicants amended claims 5, 6, 11, 15, 16, 19, and 27 in independent form to include all of the limitations of the base claim and all intervening claims.
6. The following is an examiner's statement of reasons for allowance.
7. The claimed invention pertains to the retrieving of state configuration from a state server of a hardware/software co-simulation.

8. The closest relevant prior art used is:

   - Hellestrand et al. U.S. Patent 6,263,302 ("**Hellestrand**").

9. In regards to Claim 5, Hellestrand teaches the following limitations:

> 5. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:
>
> simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
>
> (See Hellestrand, especially: Fig.1 and col.10, lines 15-35)
>
> Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).
>
> Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).
>
> Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."
>
> simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
>
> (See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)
>
> Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).
>
> Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).
>
> Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."
>
> a first kernel managing access to the memory store; and

(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single

line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following claimed limitation (emphasis added) of:

registering the client with a co-simulation interface, ***wherein registering the client comprises assigning the client a client identifier.***

10. In regards to Claim 6, Hellestrand teaches the following limitations:

6. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
(See Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

> Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following claimed limitation (emphasis added) of:

> ***wherein associating the client with at least one state server comprises providing the client with a list of available state servers and one or more address spaces associated with each of the available state server.***

11. In regards to Claim 11, Hellestrand teaches the following limitations:

> 11. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:
> simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
> (See Hellestrand, especially: Fig.1 and col.10, lines 15-35)
>
> Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).
>
> Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following set of claimed limitations (emphasis added) of:

wherein requesting the state configuration information comprises:

receiving a client identifier for the client at a co-simulation interface;

issuing a request from the co-simulation interface, said request including the client identifier and the identifier for the address space.

12. In regards to Claim 15, Hellestrand teaches the following limitations:

15. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

(See Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

(See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and

(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single

line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following set of claimed limitations (emphasis added) of:

reading the server state;

modifying the server state;

receiving the server state at a predetermined future time; and

receiving notification upon a predetermined action on the server state.

13. In regards to Claim 16, Hellestrand teaches the following limitations:

> 16. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:
>
> simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
>
> (See Hellestrand, especially: Fig.1 and col.10, lines 15-35)
>
> Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).
>
> Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).
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> Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."
>
> simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
>
> (See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following set of claimed limitations (emphasis added) of:

generating a request for the memory operation, said request including a memory allocation from the state configuration information;

accessing a memory map; and

issuing the memory operation to a unified memory for the hardware/software co-simulation based on the memory allocation and the memory map.

14. In regards to Claim 19, Hellestrand teaches the following limitations:

19. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:
simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

(See Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation,
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following set of claimed limitations (emphasis added) of:

Wherein the stimulus comprises data to be injected into the hardware/software co-simulation in response to a predetermined condition associated with the server state.

15. In regards to Claim 27, Hellestrand teaches the following limitations:

27. (Newly Amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

(See Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

(See Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(See Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(See Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

registering the client with a co-simulation interface;
(See Hellestrand, especially: col.10, lines 4-14)

and associating the client with at least one state server in the hardware/software co-simulation.
(See Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware

simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

Moreover, according to text at col.8, lines 29-31 and col.32, line 54 to col.33, line 60, Hellestrand teaches that "Fig.5 shows a flow chart of the single line parsing step according to an embodiment of the invention [in the Hellestrand patent]." Hellestrand also teaches at col.33, lines 5-7 that "The function lookup returns any timing delay adjustment (in cycles) necessary for the specific instruction to the timing obtained via the table lookup.

However, Hellestrand does not expressly teach the following set of claimed limitations (emphasis added) of:

accessing a plurality of memory locations based on the plurality of memory addresses corresponding to the server state;

assembling a plurality of data bits occupying the plurality of memory locations; and

interpreting the assembly of the plurality of data bits based at least in part upon the symbol type.

16. All dependent claims are also allowed. Claims 7-8 depend from independent claim 6. Claims 12-13 depend from independent claim 11. Claims 17, and 31-32 depend from independent claim 16. Claims 28-30 and 33-42 all depend, either directly or indirectly, from independent claim 5.

17. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

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or hand carried to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
February 3, 2006

Paul L. Rodriguez 2/6/06
Primary Examiner
Art Unit 2125